Integrated Circuit Systems, Inc.

ICS1399

T-77-13

Digital Sound Generator (DOCII)

A

General Description

The ICS1399 (DOCII) is a wave-table-lookup music synthesizer intended for use in professional keyboard instruments and other high-performance microprocessor controlled applications. This new chip achieves a new level of audio fidelity performance. These improvements are achieved through the use of waveform data interpolation and on board real time digital filters. All calculations in the device are made with at least 16-bit accuracy.

Theory of Operation

The ICS1399 (DOCII) operates in a separate memory space called sound memory. The sound memory space can be up to 1 Mbyte of 13-bit ram. The DOCII communicates to the microprocessor through its 16-bit data bus and 4-bit address bus. The DOCII contains 25 independent voices each of which is controlled by 16 voice-specific registers and 4 global registers. The DOCII creates sound for each voice in succession by performing the following algorithm: The 20-bit integer portion of the 29-bit accumulator is placed on the Address Bus (A0 thru A19). The sample data S1 is received from the Data Bus and placed in a temporary holding register. The accumulator is then incremented by one and placed on the Address Bus. This sample, S2, is used with the previous sample, S1, to compute SF, the actual sample. The value SF is now transferred to the filter computation section. In this section a real time 4 pole digital filter is implemented as 4 one pole filters cascaded in a chain. The second two poles are fixed as low pass filters, but they can be set independently as either high pass or low pass.

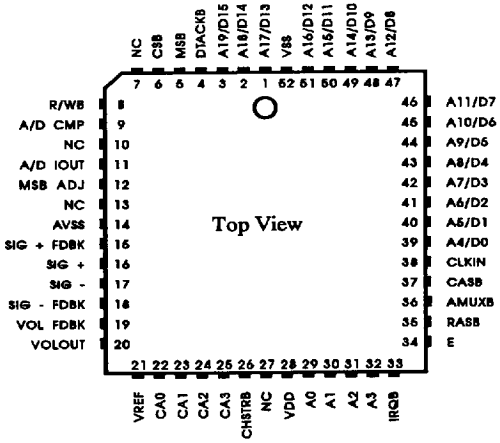
The address generation for each voice consists of a 29-bit Voice Accumulator, a Loop Start Register, a Loop End Register, and a Control Register. The Voice Accumulator contains a 20-bit integer portion and a 9-bit fractional portion. The integer portion of the Voice Accumulator is used to address the external sound ram, while the fractional portion is used in the interpolation calculation. The Control Register is used to control interrupts, the various modes of looping, and stopping and starting the voice.

The four global registers are used to set the total number of active voices, the Voice Interrupt Vector, the A-to-D Converter, and the Page Register.

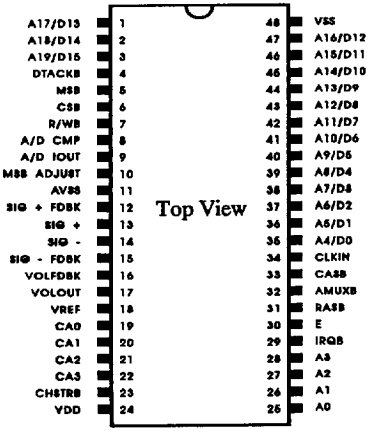
Features

- ON CHIP REAL TIME DIGITAL FILTERS
- WAVEFORM DATA INTERPOLATION
- 25 INDEPENDENT VOICES
- LOOP START AND STOP POSITIONS FOR EACH VOICE
- BI-DIRECTIONAL AND REVERSE LOOPING
- 68000 COMPATIBILITY FOR ASYNCHRONOUS BUS COMMUNICATION
- ON BOARD DIGITAL-TO-ANALOG CONVERSION
- ON BOARD 13-BIT ANALOG-TO-DIGITAL CONVERTER
- UP TO 10 MHz OPERATION
- 48-PIN DIP PACKAGE
- 52-PIN PLCC PACKAGE

ICS1399



ICS1399V - 52-Lead Plastic Leaded Chip Carrier



ICS1399N - 48-Lead Plastic DIP

Pin Descriptions

The following section describes the function of each pin of the ICS1399. The pins of the chip can be divided into five functional categories: (1) clocks, (2) control, (3) address/data transfer, (4) analog control, and (5) analog outputs. Figure 1 shows the digital waveforms and their timing relationships.

CLOCKS

CLKIN The CLKIN pin is the input clock for the DOCII. The clock can be any frequency from 1 Mhz to 10Mhz. The clock input should be as close to 50-50 duty cycle as possible, since the chip times events on both input clock edges.

RASB The RASB pin is an output pin which generates a clock used to strobe the row address information into dynamic rams. This clock occurs whenever the DOCII fetches data from memory (E clock low), or when the Memory Select (MSB) input line is low and the E clock is high. The RASB clock is high for one clock cycle and low for three clock cycles.

CASB The CASB pin is an output pin which generates a clock used to strobe the column address information into dynamic rams. This clock occurs whenever the DOCII fetches information from memory (E clock low), or when the MSB input is low and the E clock is high. The CASB clock is high for two clock cycles and low for two clock cycles.

AMUXB The AMUXB pin is an output pin which generates a clock used to multiplex the row addresses and column addresses to the dynamic ram. The AMUXB line is generated whenever RASB and CASB occurs. This clock is high for 1.5 clock cycles and low for 2.5 clock cycles which means it occurs exactly between the RASB falling edge and the CASB falling edge.

E The E clock is an output used to indicate the current state of the DOCII chip. The DOCII uses a shared bus structure: when the E signal is low, the DOCII accesses memory for sound generation; and when E is high, the DOCII and the sound memory are available for access by the processor. The E clock is high for four clock cycles and low for four clock cycles. E is normally used to enable tri-state buffers and gate the direction of data and address information to the dynamic memory. Note that even though the system shares memory, the CSB, MSB and DTACKB lines create a simple asynchronous bus communication environment.

CONTROL

R/WB The R/WB pin is an input that controls the direction of the data transfer between the DOCII and the processor. When R/WB is low, the processor is writing data into the DOCII. The R/WB line is strobed at the rising edge of the E clock; and if the CSB line is low, the DOCII will respond to the read/write request. The setup time for R/WB is 0 ns, and the hold time after the rising edge of E is 100 ns.

CSB The CSB (Chip Select) pin is an input used to select the DOCII for a read or write operation. The CSB line is strobed at the rising edge of the E clock; and if the CSB line is low, the DOCII will perform the operation requested by the R/WB signal and generate a DTACKB signal. The setup time for CSB is 0 ns, and the hold time after the rising edge of E is 100 ns.

MSB The MSB (Memory Select) pin is an input used to assist in the processor access of shared dynamic memory. The MSB line is strobed at the rising edge of the E clock. The setup time is 0 ns, and the hold time is 100 ns after the rising edge of the E clock. When the MSB line is low, the DOCII will generate RASB,CASB,AMUXB and DTACKB during an E clock high cycle.

ICS1399

DTACKB The DTACKB pin is an open drain output used to synchronize the transfer of data between a 68000 microprocessor and the DOCII or memory. The DTACKB signal will go low during an E clock high cycle whenever the CSB or MSB line is low at the rising edge of the E clock. The DTACKB line goes low two clock cycles after the rising edge of the E clock and will release at the falling edge of the E clock.

IRQB The IRQB pin is an open drain output used to signal the processor that a special case has occurred that requires servicing. The line will go low when the interrupt is required by a particular voice. When the processor reads the Voice Vector register, the line will then be released.

ADDRESS/DATA TRANSFER

A0 - A3 These four bi-directional lines are used for two purposes, determined by the state of the E clock. When E is high, these pins are used as inputs and allow the processor to access any of the data registers in the DOCII. These address inputs must be valid 100ns after the rising edge of the E clock and are latched at the falling edge of DTACKB. When E is low, these address lines are outputs used to address the external sound ram. These pins will output the voice address at the falling edge of the E clock. The address will remain valid until the falling edge of CASB, at which time the pins will go to tristate.

A4/D0 - A19/D15 These 16 lines are bi-directional and perform the data transfers from the processor or memory to the DOCII. The function of this bus depends on the state of the E clock. When the E clock is low, these lines are first used to output the address for the sound memory access. The lines A0 through A3 together with A4 through A19 form the entire 20-bit address generated by the DOCII. The addresses A4 through A19 will turn on 50 ns after E goes low and are valid 35 ns prior to the fall of RASB. The address will remain valid until the fall of CASB, at which time the bus will go to the input mode to accept the data from the memory (D0 through D15). When the E clock is high, these 16 pins are used for data transfer only. If the CSB is low and the R/WB line is high at the rising edge of the E clock, then the chip will output the data from the register requested on pins A0 through A3. If both the CSB and the R/WB lines are low then the chip will accept the data from the bus and write it into the register specified by A0 through A3. The data is latched into the chip on the falling edge of the E clock.

ANALOG CONTROL

CHSTRB The Channel Strobe pin is used to latch or sample the analog output voltage which is generated for each voice. This signal is low active and normally used to strobe a CMOS analog mux. CHSTRB is low for eight clock cycles and high for 8 clock cycles. The analog voltage will begin to change 50 ns after the rise of CHSTRB.

CA0 - CA3 The Channel Assign lines 3 through 0 are used to route or assign a particular voice to a given sample and hold or output filter. These four signals are usually tied to the select lines of a CMOS analog mux and along with CHSTRB will route the analog voltage to a particular output or position in a stereo field.

A/D CMP The Analog-to-Digital Compare pin is the serial input to a built-in successive approximation register. This input is based on a comparison of the actual analog voltage and the output of the Digital-to-Analog ladder. Each comparison for the 13-bit successive approximation register requires 16 clock cycles. A recommended circuit for the application of the A-to-D converter is shown in Figure 2. This circuit uses a sample and hold op amp strobed with the CA3 line. The sampled voltage generates a current that is compared to the A/D IOUT current. The comparison is used by the logic to generate the next A/D IOUT current approximation.

ANALOG OUTPUTS

VOLFDBK The Volume Feedback pin is a resistor connected from the VOLFDBK pin to the VOLOUT pin. This resistor is used to form the feedback resistor in a current-to-voltage op amp configuration. It is normal to adjust the response of the op amp with an external capacitor across this resistor as shown in Figure 2. The value of this resistor is approximately 4500 ohms. Note that this pin is also the reference voltage for the waveform (SIG) DAC.

SIG + FDBK The Signal + Output Feedback pin is a resistor connected from the SIG + FDBK pin to the SIG + pin. This resistor is used to form the feedback resistor in a current-to-voltage op amp configuration. It is normal to adjust the response of the op amp with an external capacitor across this resistor as shown in Figure 2. The value of this resistor is approximately 4500 ohms.

SIG - FDBK The Signal - Output Feedback pin is a resistor connected from the SIG-FDBK pin to the SIG- pin. This resistor is used to form the feedback resistor in a current-to-voltage op amp configuration. It is normal to adjust the response of the op amp with an external capacitor across this resistor as shown in Figure 2. The value of this resistor is approximately 4500 ohms.

A/D Iout The Analog-to-Digital Current Output pin is the output of the successive approximation register converted to a current. It is a 13 bit ladder which has an LSB step of approximately 200μA. It is important that this node not exceed -0.5 volts in any configuration; therefore, protection diodes should be used. For proper operation, this output should be an op amp "virtual ground."

VOLOUT The Volume Output pin is a current output signal which represents the analog value of the data stored in the volume register for each voice. This signal, in conjunction with the VOLFDBK pin, is used with an op amp to create a negative volume voltage.This voltage is then applied to the Signal DAC so that an analog multiplication is performed. The circuit configuration for the current-to-voltage convert is shown in Figure 2. The Volume DAC is a 12 bit ladder which has an LSB step of approximately 400μA. For proper operation, this output should be an op amp "virtual ground."

SIG+, SIG- The two Signal output pins represent a differential current output of the final analog signal generated for each voice by the DOCII. These signals are each used in a current to voltage configuration using the SIGFDBK pins and then the voltage outputs are combined in a differential amplifier to create the final analog output voltage for a voice. This information can then be routed through an analog multiplexer to its final destination. The entire recommended configuration is shown in Figure 2. For proper operation, these outputs should be op amp "virtual grounds."

VREF The VREF pin a supply voltage used to power the resistor ladders and drivers for the DACs in the DOCII. This supply should be as low noise as possible since any noise on this supply will appear in the final output or input sample. The nominal voltage is 5 volts and the input impedance is approximately 1800 ohms.

AVSS The AVSS pin is an analog ground pin. This ground is used in the DOCII for the ground return of the Volume and A to D converter ladders. It is important that this ground be as low noise as possible since any noise on this line will be injected into the DACs.

MSB Adjust This pin is used to trim the waveform DAC zero crossing to achieve minimum noise and distortion. See Figure 2.

The following section describes in detail the structure and purpose of each of the registers in the DOCII chip. All unused bits in a register will read back as logic one.

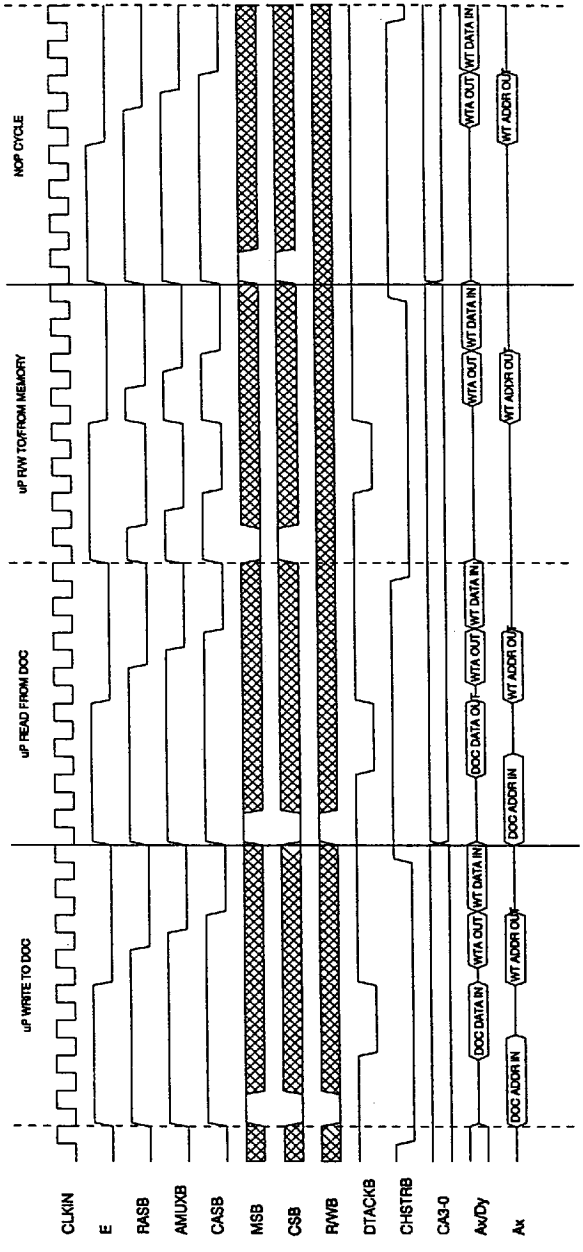


Figure 1: Timing Diagram

The Global Registers

Page Register - $F

The Page Register is used to access the set of 16 registers which control all aspects of a voice. The Page Register appears at location F hex in all pages. There are a total of 64 pages which can be accessed through the Page Register. Locations 0 through A hex of pages 0 to 24 control the most often used settings for each voice. Locations 1 through 6 of pages 32 to 56 offer access to the temporary registers for the intermediate data used in the real time filter calculations.

Voice Interrupt Vector Register - IRQV - $E

The Voice Interrupt Vector register is used by the microprocessor to determine which voice has caused an interrupt to occur. When a voice has its interrupt enabled in its corresponding control register and the proper events occur to cause an interrupt to be issued, the voice number is placed into this register so that the processor can read the value and determine which voice requires servicing. The IRQ output line of the DOCII chip will go high after the processor reads this register. Bit 7 of this register is a monitor of the IRQ output line, and bits 4 through 0 determine the voice interrupt. Conditions sufficient to cause an interrupt will be defined in the Interrupt Control Section.

Active Voice Register - ACT - $D

The Active Voice Register defines how many voices are actually enabled to produce sound. This register uses bits 4 through 0, encoding values 24 through 0. The actual number of active voices is equal to the number in this register plus one. The number of active voices determines the output sample rate of the DOCII. Each voice takes 1.6 microseconds to be processed if the DOCII is running at 10MHz. When all 25 voices are active, this corresponds to a 25KHz sample rate. If only 16 voices are active, the sample rate is 39KHz.

A-to-D Converter - A/D - $C

The DOCII has a built in 13 bit A-to-D Converter. It is a successive approximation converter which requires 1.6 microseconds per bit plus one for a complete conversion. If the full 13 bit accuracy is required, the sample rate of the converter is 44.6 KHz, which is 14 times 1.6 microseconds. The conversion period is determined by setting the start sample bit in one of the voice control registers. For example, if there are 16 active voices and the start sample bit is set in voice zero, then a new conversion will start every time voice zero is processed; therefore, the conversion rate is 39KHz. If the number of active voices is now reduced to 14, then the maximum conversion rate will be achieved. If the conversion rate is set below 14 voice times, then the actual number of bits accurately converted is equal to two less than the number of voices between start sample commands issued. If there are 24 active voices and the start conversion bits are set for voices 0 and 12, then two 9-bit conversions are performed during one total voice cycle.

The output register of the A-to-D converter is buffered such that the result of a conversion is available while the next conversion is being performed. The processor must retrieve the information from the output register before the next conversion is completed. The A-to-D Converter Register also contains two additional bits which are used for testing. Bit 0 of this register, when set to a one, divides all the D-to-A ladders on the chip in half. This allows the resolution requirements for testing to be kept at a reasonable level. The 13-bit D-to-A ladders are divided into a 7-bit section and a 6-bit section. The lower portion of the divided ladder is connected to VDD when bit 0 is a one.

Bit 1 of the A-to-D Register is used to test the D-to-A ladder used in the A-to-D conversion process. When this bit is set to a one, the upper 13 bits of the A-to-D register can be written to by the processor. This allows the ladder to be tested as a standard D-to-A converter. This ladder is also split in two by bit 0 and the A-to-D register.

The Voice Specific Registers

The following section describes the registers which control a voice in the DOCII. The registers for a specific voice are accessed using the A3-A0 address lines. The page register is used to direct the data flow to a particular voice. All bits in all the voice specific registers can be written to and read from. Note that the register name and the abbreviation in parentheses which follows it may be used interchangeably.

ICS1399

The Control Register (CR) - $0

The Control Register is an 8-bit register which directs various aspects of the DOCII. The following is a list of control register bits and their function:

IRQ A status flag shows that this voice has requested service through the Voice Interrupt Vector or has an interrupt request pending and is waiting for the Voice Interrupt Vector to be cleared of the current voice.

DIR This bit indicates the direction the sample is being scanned by the address ALU. A zero indicates the forward (incrementing) through memory; a one indicates the decrementing case. If the bi-directional looping mode has been selected, the address ALU will automatically toggle this bit when the address reaches either the Loop Start or Loop End positions.

IRQE This bit enables the Interrupt for the voice if IRQE = 1.

BLE Bi-directional looping is enabled if BLE = 1 and LPE = 1.

LPE Looping is enabled if LPE = 1. Looping refers to restoring the address accumulator to the Loop Start position when the address accumulator exceeds the value in the Loop Stop register. If the LPE bit is a zero, then the accumulator will stop when it reaches Loop Stop. The role of the Start and Stop positions is reversed if the DIR bit is a one. The state of BLE is ignored if LPE = 0.

A/D Start A to D Conversion when this bit is set to a one. A new conversion will start each time this voice is processed.

STOP1 This bit is used by the processor to stop the address ALU from modifying any bits in a voice during its normal processing. For example, if this bit is set, then the newly calculated address for the next sample will not be stored into the address accumulator or the direction bit will not be changed. This feature allows the microprocessor to change the contents of either the control register or accumulator without concern.

STOP0 This bit performs the same function as the STOP1 bit. The difference is that this bit can be set by the address ALU. This bit is set when Looping is disabled and the accumulator reaches the Loop Stop position. Note that both STOP1 and STOP0 must equal zero for the voice to run.

The Frequency Control Register (FC) - $1

The Frequency Control Register is used to define the rate at which the address ALU will step through the sample memory. The register is a 15-bit word, left justified, that is divided into a 6-bit integer portion and a 9-bit fractional portion. At 10Mhz operation this yields an effective 2 cents resolution.

The Start Registers (STRT) - high = $2, low = $3

The Start Register, also called the Loop Start Register, is a 24-bit value divided into two register locations, namely registers 2 and 3. Register 2 contains the upper 13 bits of the Loop Start position, while register 3 contains the lower 11 bit of the position. The upper 13 bits are right justified and lower 11 bits are left justified (See Register Map). The Loop Start position, as its name implies, is used to define where in the sample memory the accumulator will jump to when it reaches the Loop End position. Note that the Loop Start register has a 20-bit integer portion and a 4-bit fractional nibble. This fractional positioning capability allows much finer frequency resolution tuning when looping a waveform.

The End Registers (END) - high = $4, low = $5

The End Register, also called the Loop End Register, is partitioned the same way as the Start Register, a right justified 13-bit MSW and a left justified 11-bit LSW. It is used to mark the end of a loop in the sample memory. Note that the Start and End Registers reverse their roles if the Direction bit is a one. The End register contains the same integer and fractional partition as the Start register.

Filter Cutoff High (K2) - $6

The Filter Cutoff High Register is used to determine the 3dB point of poles three and four of the digital filter. It is a 12-bit register, left justified, using bits 15 through 4.

Filter Cutoff Low (K1) - $7

The Filter Cutoff Low Register is used to determine the 3dB point of poles one and two of the digital filter. It is a 12-bit register, left justified, using bits 15 through 4. See the later section on the digital filter for calculations of the coefficient values.

Volume (VOL) - $8

The Volume Register is a 12 bit left justified register used to define the effective amplitude of the sampled signal. The information stored in this register is applied to the Volume D to A converter at the same time the sample data is applied to the waveform D to A converter. The Volume information is converted to a voltage by an external current-to-voltage converter and this resultant voltage becomes the reference supply for the waveform D to A. This configuration performs an analog multiplication of the Volume data and the interpolated Sample data.

Channel Assign/Filter Configuration - $9

This register is used to define the 4-bit output channel information and the digital filter configuration. Bit 3 through 0 specify the channel and bits 4 and 5 specify the filter mode. The Channel Assign information is a 4-bit code normally used to specify an output channel for the current voice. For example, the code could be used to control an analog multiplexer which is weighted to provide a stereo pan. This would allow up to sixteen possible left to right weightings for the voice. Additionally, one could set up separate outputs beyond the two used for stereo, and that voice could then be routed directly to one specific output. Up to 16 separate outputs can be defined in this manner. It is possible, with the use of external latches, to use the Channel Assign lines as address bank switches allowing the DOCII to address additional memory banks. The Filter Configuration bits define the four possible modes of the digital filter. The two bits used are referred to as LP4 and LP3, which are lowpass pole 4 and lowpass pole 3, respectively. The following chart indicates these configurations:

Filter Configuration and Coefficient Assignments

LP4	LP3	Filter Pole 4/ Coefficient	Filter Pole 3/ Coefficient
0	0	HP/K2	HP/K2
0	1	HP/K2	LP/K1
1	0	LP/K2	LP/K2
1	1	LP/K2	LP/K1

Note that the above chart shows both the mode of the filter pole as well as the coefficient value used in the filter computation. In the digital filter poles, one and two are always low pass and always use coefficient K1.

Accumulator (ACCH/ACCL) - High/Low - $A/$B

The Accumulator is a 29 bit register divided into two parts, Accumulator High and Accumulator Low. The Accumulator High is 13 bits right justified (ACCH12 through ACCH0) and the Accumulator Low is a full 16-bit word (ACCL15 through ACCL0). The Accumulator is comprised of an integer portion and a fractional portion. The integer part is 20 bits using ACCH12-ACCH0, ACCL15-ACCL9. This 20-bit value is the actual information used to fetch the sample data from memory. The 9-bit fractional part is needed to obtain proper frequency resolution and also for the interpolation calculation to be discussed in the Signal Processing section. The Accumulator is also used as the waveform start position. This is not to be confused with the use of the Loop Start register. The initial Accumulator value is the beginning of the waveform while the Loop Start position defines the beginning of the sustain part of the waveform.

The Filter Storage Registers

Pages 32 through 57 are used to address six Filter Storage Registers in each voice. These registers are used as temporary storage location for the real time digital filters in each voice. Each digital filter requires six 16-bit registers to complete its calculations. These six registers are addressable by the processor mainly for testing purposes and initialization, but there may be some yet-to-be-determined audio benefits achieved by some real time processor intervention. Note that when accessing these pages, the global registers are still available.

Filter Pole 4(n-1) - $1

A 16-bit register containing the last output of the final stage of the digital filter. This register is the actual data that is presented to the signal D to A converter.

Filter Pole 3(n-2) - $2

A 16-bit register which records the output of the third stage of the digital filter from the previous sample time. This information is needed to process the high pass filter mode of filter pole 4.

Filter Pole 3(n-1) - $$3

A 16-bit register containing the last output of the third stage of the digital filter. The output of this stage becomes the input to the fourth stage and the data pushed into Pole 3(n-2) on the next cycle.

Filter Pole 2(n-2) - $4

A 16-bit register which records the output of the second stage of the digital filter from the previous sample time. This information is needed to process the high pass filter mode of filter pole 3.

Filter Pole 2(n-1) - $5

A 16-bit register containing the last output of the second stage of the digital filter. The output of this stage becomes the input to the third stage and the data pushed into Pole 3(n-2) on the next cycle.

Filter Pole 1(n-1) - $6

A 16-bit register containing the last output of the first stage of the digital filter. The output of this stage becomes the input to the the second stage.

ICS1399

The Register Map

Pages 0 through 24

Reg	Symbol	Description	Bits Justification
0	CR	CONTROL REGISTER	8[7:0]
1	FC	FREQUENCY CONTROL	15[15:1]
2	STRT-H	LOOP START REG - HIGH	13[12:0]
3	STRT-L	LOOP START REG - LOW	11[15:5]
4	END-H	LOOP END REG - HIGH	13[12:0]
5	END-L	LOOP END REG - LOW	11[15:5]
6	K2	FILTER CUTOFF COEFFICIENT #2	12[15:4]
7	K1	FILTER CUTOFF COEFFICIENT #1	12[15:4]
8	VOL	VOLUME	12[15:4]
9	CA	FILTER CONFIG/CHANNEL ASSIGN	6[5:0]
10	ACCH	ACCUMULATOR HIGH	13[12:0]
11	ACCL	ACCUMULATOR LOW	16[15:0]
12	A/D	A TO D CONVERT / TEST	16[15:0]
13	ACT	NUMBER OF VOICES	5[4:0]
14	IRQV	INTERRUPTING VOICE VECTOR	5[4:0]
15	PAGE	PAGE SELECT REGISTER	6[5:0]

Pages 32 through 56

Reg	Symbol	Description	Bits Justification
1	O4(n-1)	FILTER 4 TEMP REGISTER	16[15:0]
2	O3(n-2)	FILTER 3 TEMP REG #2	16[15:0]
3	O3(n-1)	FILTER 3 TEMP REG #1	16[15:0]
4	O2(n-2)	FILTER 2 TEMP REG #2	16[15:0]
5	O2(n-1)	FILTER 2 TEMP REG #1	16[15:0]
6	O1(n-1)	FILTER 1 TEMP REGISTER	16[15:0]
12	A/D	A TO D CONVERT / TEST	13[15:3], 2[1:0]
13	ACT	NUMBER OF VOICES	5[4:0]
14	IRQV	INTERRUPTING VOICE VECTOR	5[4:0]
15	PAGE	PAGE SELECT REGISTER	6[5:0]

Definition of Specific Bits in the Multipurpose Registers

REG	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
CR	1	1	1	1	1	1	1	1	IRQ	DIR	IRQE	BLE	LPE	STRT A/D	STP1	STP0
CA	1	1	1	1	1	1	1	1	1	1	LP4	LP3	CA3	CA2	CA1	CA0
A/D	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	1	A/D R/W	LAD TEST
IRQV	1	1	1	1	1	1	1	1	IRQB	1	1	IV4	IV3	IV2	IV1	IV0

Signal Processing in the DOCII

The following section describes the data flow and algorithms used in the DOCII. To adequately explain the functions which eventually produce the final output, the architecture will be presented in three sections: address generation, sample interpolation, and digital filtering.

ADDRESS GENERATION

The DOCII uses a technique called "Phase Accumulating Counters" to achieve pitch transposition of a previously sampled waveform. This technique uses an adder, an accumulator, and a frequency control word. Each of these component pieces contains an integer and a fractional portion. At each voice time slot, the frequency control word is added to the accumulator and strobed back to the accumulator. Consider, for example, that we wish to transpose a sinewave already in memory up one-half octave. This requires that we add to the accumulator the value 1.5 at each accumulation. This calculation can certainly be performed since all the structures have a fractional portion, but the sampled data does not contain a sample 35.5 for instance, only sample 35 or 36. In order to approximate sample 35.5, we must interpolate half way between the two data points contained in samples 35 and 36. Interpolation will be discussed in the next section and is referred to here since the fractional aspect of the phase accumulating technique requires careful consideration when dealing with the looping.

In order to loop on a waveform, the following algorithm is performed.

1. Fetch the Accumulator and put integer portion of accumulator on external address bus.
2. Add 1 to Accumulator and place on external address bus. This is used for interpolation. This incremented value is not retained.
3. Add Frequency control word to Accumulator
4. Subtract Loop End from Accumulator
5. If Loop End Accumulator, then add Frequency Control to Accumulator or else add remainder of subtraction in Step 4 to Loop start.

As can be seen, the remainder of the subtraction in Step 4 is important to keep the phase of the waveform intact when looping and transposing. The counting algorithm presented here is used for all modes of looping except that the roles of the Loop Start and Loop End registers will be swapped depending on the direction of the count.

INTERPOLATION

Once two successive samples have been fetched from the sound memory, it is necessary to use linear interpolation to approximate a new sample. This approximation is done by performing the following calculation:

$$SF = S1 + ACCfr * (S1 - S2), \text{ where}$$

SF is the new sample
S1 is first sample fetched
S2 is the second sample fetched
ACCfr is the 9 fractional bits of the Accumulator.

DIGITAL FILTERING

The new sample generated by linear interpolation is ready to be filtered. Each voice in the DOCII is passed through four one pole filters. Each of these digital filters simulates a one pole Butterworth filter. As previously mentioned in the discussion of the filter configuration bits in register 9, filters one and two are fixed as low pass and filters three and four are selectable as either low pass or high pass. The table shown previously describes the four possible filter configurations and how the filter coefficients are applied.

The filter coefficients K1 and K2 are used to define the cutoff frequency of the filter. The following set of equations shows the set of calculations performed on the sample data stream for each voice. The low pass filter is modeled by:

$$Y_n = K*(X_n - Y_{n-1}) + Y_{n-1}, \text{ where}$$

Y is the new output
K is the cutoff coefficient
X is the input
Y is the previous output

The high pass filter is modeled with:

$$Y_n = X_n - X_{n-1} + K * Y_{n-1}, \text{ where}$$

Y is the new output
K is the cutoff coefficient
X is the input
X is the previous input

The four filters are cascaded such that the output of the first is the input to the second and so on.

ICS1399

The coefficients K1 and K2 define the cutoff frequency of the filters. Given a desired attenuation (normally the -3dB point) the value for K can be determined from the following relationship for the low pass filter. Note that K is always a number less than 1.

$K = \{1-\cos(w)-\sqrt{[\cos^2(w) + (2/N^2)*[1-\cos(W)1]}\}/[(1/N^2)]$, where

K is the cutoff coefficient,
$W = 2\pi f$, where f = frequency of interest and F is the sampling frequency,
N is the attenuation factor, .707 for -3dB.

A similar relationship can be developed for the high pass filter.

$K = \{\cos(W)-\sqrt{[\cos^2(w) + (2/N^2)*[1-\cos(W)]-1}\}$, where

K is the cutoff coefficient,
$W = 2\pi f$, where f = frequency of interest and F is the sampling frequency,
N is the attenuation factor, .707 for -3dB.

The most useful range of a high pass filter is generally below 4kHz. In order to maximize the resolution of the filter in that range an offset of .5 has been added to the K coefficient. This offset means the highest cutoff frequency achievable is approximately 800 Hz for one high pass pole.

To determine the 12 bit digital value required for the K register, perform the following calculation. For the low pass filter, multiply the value obtained from the previous equation by 4096. For the high pass filter subtract 0.5 and multiply by 8192.

Remember that the equations presented here are for one pole only, and the value for the attenuation factor N must be scaled for the number of poles. For a one pole filter the 3dB point means N is equal to .707; a two pole filter requires each one pole filter to have N equal to .84; a three pole and N equals .89, etc.

Interrupt Handling in the DOCII

An interrupt can be caused by any active voice in the DOCII. A voice will request interrupt servicing when the interrupt enable bit has been set and the accumulator has reached the loop end point (loop start if the direction bit is set). An interrupt will be issued by a voice regardless of the state of the loop mode bits when the accumulator reaches the loop end. When an interrupt has been requested, the interrupt bit (bit 7 in the Control Register) is set, the voice number is latched into the Voice Interrupt Vector register, and bit 7 of the Voice Vector register is cleared low. When the processor reads the Voice Vector register, bit 7 of the Voice Vector register is set high and when the voice which caused the interrupt is next processed, bit 7 of its Control Register is cleared. If a voice has reached an interrupt condition and the Voice Vector already contains information from another voice, that new voice interrupt request will be stacked. This stacking occurs automatically since the interrupt bit in the Control Register of the voice will be set when the interrupt condition occurs. Eventually the processor reads the Voice Vector clearing the old interrupt vector information, and the new vector will be placed in the register when the new voice is again processed. Note this ability allows the processor to force an interrupt from a voice simply by setting the interrupt enable bit and the interrupt bit of a particular voice. Due to a design oversight a special procedure must be performed to insure proper initialization of the Interrupt Vector Register. The Voice Vector Register is 5 bits and can power up with a value greater than 24. Since there are only 25 voices this is an invalid condition. In order to correct this situation it is necessary to perform the following. First, set the number of active voices to 32 (value 1F in reg D). Second, set the interrupt bit and interrupt enable bits of voices 0, 1, and 2. Third, continuously read the Vector register until either a 0 or 1 occurs. Fourth, set the number of active voice to a valid number, 25 or less. Fifth, clear all remaining valid interrupts by clearing the interrupt and interrupt enable bits for all voices.

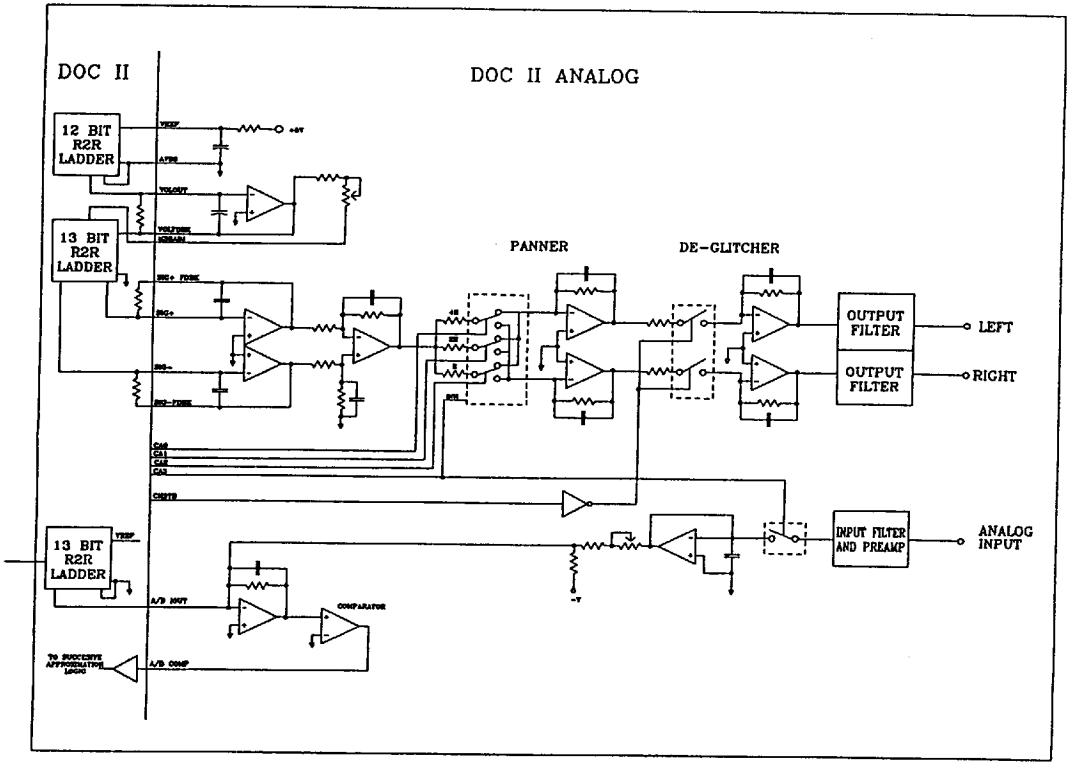


Figure 2 Typical Application Analog Block Diagram